



PTO/SB/08A (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known

Application Number	10/760,549
Filing Date	January 21, 2004
First Named Inventor	Masayoshi TONOUCHI
Art Unit	2829
Examiner Name	J.M. HOLLINGTON
Attorney Docket Number	ASAIN0137

FOREIGN PATENT DOCUMENTS						
Examiner Initials ^a	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ^d
		Country Code ³ Number ⁴ Kind Code ³ (if known)				
J. M. H. ↓	A	JP 2000-036525	02-02-2000	NEC Corp.	_____	
	B	JP 2000-311929	11-07-2000	NEC Corp.	_____	

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Translation is attached.
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
J. H.	C	Kiyoshi NIKAWA, "Failure Analysis in Si Device Chips." IEICE Trans. Electron, Vol. E77-C, No. 4, April 1994, pp. 528-534.	
	D	Hideo TODOKORO et al., "Electron-Beam LSI Tester." In "Semiconductor Technologies," J. Nishizawa (ed), Vo. 13, JARECT, 1984, pp. 373-382.	
↓	E	David H. AUSTIN et al., "Electrooptic Generation and Detection of Femtosecond Electrical Transients." IEEE J. Quantum Elec., Vol. 24, , No. 2, February 1988, pp. 184-197.	

Examiner Signature	<i>J. H.</i>	Date Considered	8/2/05
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